Page 22, line 16, change "Techniques." to --Techniques,"
Serial No. 07/337,579, filed April 13, 1989, now abandoned.--

Page 26, line 3, insert a comma --,-- after "204,175" and insert thereafter --now patent no. 5,095,344,--.

Page 26, strike all of line 64, and substitute the following therefore: --Harari, Serial No. 07/337,579, filed April 13, 1989, now abandoned,--.

IN THE CLAIMS:

Cancel claims 1-62, without prejudice, and substitute the following new claims 63-89 therefor:

--63. A Flash EEprom system comprising:

one or more integrated circuit chips each having an array of Flash EEprom cells partitioned into a plurality of sectors, each sector addressable for erase such that all cells therein are erasable simultaneously, the cells of the array being individually programmable into more than two states in order to store more than one bit of data per cell;

means for selecting a plurality of sectors among the one or more chips for erase operation;

means for simultaneously performing the erase operation on only the plurality of selected sectors; and

individual register coupled ~~associated~~ with each sector for holding a status to indicate whether the sector is selected or not.

64. The Flash EEprom system according to claim 63, wherein the simultaneously erasing means is responsive to the status in each of the individual registers, such that only the selected sectors are included in the erasing.

65. The Flash EEprom system according to claim 63, wherein any one or combination of the individual registers indicating a selected status are individually resettable to an unselected status.

66. The Flash EEprom system according to claim 63, wherein all the individual registers are simultaneously resettable to a status indicating the associated sectors as not selected.

67. A method of operating a memory system having an array of EEPROM cells divided into multiple non-overlapping sectors that individually contain a plurality of said cells sufficient to store multiple bytes of data and which are erasable together, comprising:

(a) initially tagging a plurality of said multiple sectors to be erased,

(b) subjecting the EEPROM cells of the tagged sectors in parallel to erase voltages while the remaining multiple sectors are not so subjected,

(c) thereafter verifying whether individual ones of the tagged sectors have become erased,

(d) clearing the tags from those sectors which are verified to have become erased while continuing to subject remaining tagged sectors to erase voltages,

(e) repeating operations (b) through (d) until the tags have been cleared from all of the initially tagged sectors, thereby to erase all the initially tagged sectors, and

(f) programming the individual cells of the array into one of more than two programmable states in order to store more than one bit of data per cell.

68. The method of claim 67, which additionally comprises maintaining an identification of those of said multiple sectors that are defective, and avoiding subjecting such identified sectors to the erase voltages.

69. The method of claim 67, which additionally comprises limiting the number of sectors that are erased in parallel in response to a predetermined power capability of the memory system.

70. The method of any one of claims 67-69 wherein operation (a) includes initially tagging a plurality of but less than all of said multiple sectors to be erased.

71. A flash EEPROM system, comprising:

a memory controller and system address bus,

multiple sectors of flash EEPROM cells ~~that are~~ individually addressable through said address bus to be erased and

which individually store multiple bytes of data, the cells of the individual sectors being erasable together when the individual sectors are addressed, the cells of the system being individually programmable into more than two states in order to store more than one bit of data per cell,

a logic circuit coupled to said multiple sectors and configured to address and enable for erasure, in response to signals from the controller, any combination of a plurality of but less than all of said multiple sectors, and

an erase circuit coupled to said multiple sectors to erase together all the enabled sectors without erasing others of the multiple sectors that are not so enabled.

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72. The system of claim 71, wherein the logic circuit includes a register associated with individual ones of the sectors to tag its respective sector as enabled for erasure.

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73. The system of claim 72, which additionally comprises a verifying circuit that indicates when individual sectors have been erased, and wherein the logic circuit is responsive to said verifying circuit for clearing tags from those registers of a particular combination of sectors which are verified to be erased while maintaining the tags in the registers associated with others of said particular combination of sectors.

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74. The system of claim 71, which additionally comprises a verifying circuit that indicates when individual sectors have been erased, and wherein the logic circuit is responsive to said verifying circuit for disabling from further erase those of a particular combination of sectors which are verified to be erased while maintaining enabled for erase others of said particular combination of sectors.

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75. The system of any one of claims 71-74, wherein the erase circuit is coupled to erase all the enabled sectors in parallel.

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76. The system of any one of claims 71-74, wherein the multiple sectors of EEPROM cells include substantially all the EEPROM cells in the system.

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77. A flash EEPROM system, comprising:

multiple sectors of flash EEPROM cells that are individually addressable for erasure and which individually store multiple bytes of data, the cells of the individual sectors being erasable together, the cells of the system being individually programmable into more than two states in order to store more than one bit of data per cell,

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coupled to said multiple sectors and

a logic circuit configured to enable erasure of any one of multiple different combinations of a plurality of but less than all of said multiple sectors, and

said multiple sectors to

an erase circuit coupled to erase together all the enabled sectors of said any one combination without erasing others not in said any one combination.

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78. The system of claim 77, wherein said logic circuit includes a plurality of registers that individually contain a tag indicating whether an associated sector is enabled for erasure or not.

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79. The system of claim 78, which additionally comprises a verifying circuit that indicates when individual sectors have been erased, and wherein the logic circuit is responsive to said verifying circuit for clearing tags from those registers of a particular combination of sectors which are verified to be erased while maintaining the tags in the registers associated with others of said particular combination of sectors.

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80. The system of claim 77, which additionally comprises a verifying circuit that indicates when individual sectors have been erased, and wherein the logic circuit is responsive to said verifying circuit for disabling from further erase those of a particular combination of sectors which are verified to be erased while maintaining enabled for erase others of said particular combination of sectors.

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81. The system of any one of claims 77-80, wherein the erase circuit is coupled to erase all the enabled sectors in parallel.

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~~82~~. A method of operating a memory system having an array of EEPROM cells divided into multiple non-overlapping sectors that individually contain a plurality of said cells sufficient to store multiple bytes of data and which are erasable together, comprising:

(a) designating a combination of a plurality of but less than all of said multiple sectors to be erased,

(b) erasing the combination of sectors without erasing others of said multiple sectors,

(c) after the combination of sectors has been erased, writing data in at least some of the erased combination of sectors by programming the individual cells therein into one of more than two programmable states in order to store more than one bit of data per cell, and

(d) repeating the operations of (a) through (c) with another combination of sectors.

21 ~~83~~. The method of claim 20 ~~82~~, wherein the operation of erasing the combination of sectors includes:

verifying when individual sectors in the combination of sectors become erased,

terminating further erasing of such verified sectors while continuing to erase others of the combination of sectors, and

terminating further erasing of any of the combination of sectors when all of the combination of sectors have been verified as erased.

22 ~~84~~. The method of claim 21 ~~83~~, wherein designating the combination of sectors includes setting a tag bit for individual ones of the sectors to be erased, and wherein terminating further erasing of the verified sectors includes clearing the tag bits for the sectors which have been verified.

23 ~~85~~. The method of claim 20 ~~82~~, wherein designating the combination of sectors includes setting a tag bit for individual ones of the sectors to be erased, and wherein erasing the combination of sectors is terminated by ~~includes~~ clearing the tag bits associated with the sectors that have been erased.

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